REMARKS

Reconsideration of this application in light of the above amendments is courteously solicited.

The Examiner in the final rejection dated April 7, 2003, when responding to Applicant's arguments filed in their amendment of February 3, 2003, indicates that Applicant's arguments were not commensurate with the scope of the claims as presented. Specifically, the Examiner indicates that claim 1 does not set forth the "cache memory... implanted in a hardware manner". In response to this point, Applicant has now amended independent claim 1. Claim 1 has been amended to specifically set forth "...a sub-clip predictor for performing a hardware-based prefetch of a sub-clip to be soon needed...". The 6,417,860 patent fails to teach, disclose, suggest or render obvious the clipmap concept between a system memory and a texture cache as now claimed in amended claim 1. The '860 patent teaches a method for reducing the required capacity of system memory wherein the clipmap concept is applied into the relation between a hard disk and system memory (in this regard see Figure 2) by implementing it in an entirely software manner. This is not suitable for accelerating the texture mapping. As noted above, with respect to the present invention, a new cache memory capable of accelerating the textured mapping process is implemented in a hardware manner. Above amended claim 1 shows

elements for implementing the mapping process in a hardware manner. Accordingly, it cannot be said that the '860 patent teaches all the limitations of Claim 1 with the exception of the DRAM having a SAM port. Accordingly, it is submitted that independent claim 1 defines over the prior art.

With respect to dependent claim 4, it is submitted that dependent claim 4 contains patentable merit in its own right. Claim 4 provides a plurality of data paths for performing a trilinear interpolation in one clock cycle by accessing eight texels simultaneously. The tertiary reference to Sara applied by the Examiner teaches eight RAMs for this purpose.

The Examiner in responding to Applicant's arguments regarding the patentability of dependent claim 5 and independent claim 6 argued that neither of the claims set forth "prediction in numeral 3-dimensional space". With regard to dependent claim 5, again it is submitted that claim 5 contains patentable merit in its own right. The sub-clip predictor of the present invention is a prefetching controller (See Figure 8) for prefetching texture data predicted to be used at the next time in a 3-dimensional space considering movements of LOD level as well as in 2-dimensional space. The Park reference does not teach the prefetching of another texture data predicted to be used the next time in 3-dimensioanl space. Park teaches a prefetching controller for prefetching in 2-dimensional space.

Accordingly, it is submitted that claim 5 is patentable over the prior art.

Method claim 6 is likewise patentable over the prior art. In accordance with claim 6, the present invention discloses a method for reducing a penalty occurring upon a cache miss, the method comprising a stack layer prediction step (prediction in 3-dimensionl space) as well as a sub-clip prediction step in one stack layer (prediction in 2-dimensional space). As noted above, the secondary reference to Park teaches a method for prefetching the next texture data by using the address from the address generator based on the directional signal in 2-dimensional space. Accordingly, it cannot be said that claim 6 is rendered obvious by the teachings of the Migdal et al. reference in view of Park.

In summary, Applicants have now amended the claims in a manner commensurate with the considered arguments of the Examiner in response to Applicants previously filed amendment. Accordingly, the claim amendments made in the instant response do not raise new issues which would require further search or reconsideration on the Examiner's part as, clearly indicated in the Examiner's remarks, these points have been considered previously. Applicants have amended the claims so as to remove the Examiner's objections and to set forth with more specificity the inventive subject matter of the instant application In

light of the foregoing, it is submitted that all of the claims as pending are in condition for allowance and an early indication of same is respectfully requested.

An earnest and thorough attempt has been made by the undersigned to resolve the outstanding issues in this case and place same in condition for allowance. If the Examiner has any questions or feels that a telephone or personal interview would be helpful in resolving any outstanding issues which remain in this application after consideration of this amendment, the Examiner is courteously invited to telephone the undersigned and the same would be gratefully appreciated.

It is submitted that the claims as amended herein patentably define over the art relied on by the Examiner and early allowance of same is courteously solicited.

If any fees are required in connection with this case, it is respectfully requested that they be charged to Deposit Account No. 02-0184.

Respectfully submitted,

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By_____

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313" on June 23, 2003.

Rachel Piscitelli

Version with markings to show changes made to the claims

1. (Twice Amended) A cache memory for three-dimensional graphics texture mapping, comprising:

a first DRAM bank for storing all texels of predetermined upper levels of LOD (Level of Detail) and a second DRAM bank for storing only a working set currently needed among the remaining levels of LOD, wherein said first and second DRAM banks including SAM ports, respectively, each of said SAM ports reading a texture for a trilinear interpolation and fetching new texture sub-clips from the outside;

a sub-clip loader connected to said SAM ports of said first and second DRAM banks and for fetching new texture sub-clips from an external system memory;

a sub-clip predictor for performing a hardware-based prefetch of a sub-clip to be soon needed,

a controller for controlling said components; and

a CAM for checking if eight texels existing at an integer coordinate relative to an LOD and (u, v) coordinates are located in said first and second DRAM banks, when the LOD and (u, v) coordinates mapped into a texture space with respect to a pixel to be rendered on a display screen are input to said controller.

5.(Twice Amended) The cache memory according to claim 1, [further comprising a] wherein said sub-clip predictor [for performing a hardware-based prefetch of a] prefetch sub-clip predicted to be soon needed in a 3-dimensional space, so as to reduct a penalty due to cache miss.

6. (Amended) A method for reducing a penalty occurring upon a cache miss, comprising the steps of:

performing a sub-clip prediction in one stack layer, where, under a hardware-based sub-clip prediction limit 2 by 2 sub-clip boundary inside of sub-clips (4 by 4) one a current clip RAM stack, when the tracing of (u, v) coordinates passes the limit, sub-clips of the tracing direction (left, right, upper and lower sides) are prefetched; and

performing a stack layer prediction in 3-dimensional space, where the current clip RAM stack represents the levels of LOD (LOD I to LOD i+3_ storde in said stack, internal two levels of LOD are used as a prediction limit, and, immediately after the tracing of LOD passes the limit, a stack layer corresponding to a next level of LOD is prefetched.